Curriculum Vitae

Name	**Dr. G. Sai Saravanan**
Designation	Scientist 'G' in Defence research and development organization (DRDO)
Laboratory	SMRC, at Gallium Arsenide Enabling Technology Centre (GAETEC), Hyderabad - 500069, India
Date of birth	31.07.1966



Educational qualifications:

- M. Sc. in Physics with electronics, 1989, Bharathidasan University, Tamil Nadu
- M. Tech. in Laser & Electro-optical Engineering from College of Engineering, Anna University, Chennai, 1990 & 1992
- Ph. D. in Physics from University of Hyderabad, Hyderabad, 2008

Work experience:

- Joined as a Scientist at Solid State Physics Laboratory (SSPL), Delhi in 1991
- Working at SMRC, [a unit of Solid State Physics Laboratory (SSPL), Delhi] at GAETEC, Hyderabad, since 2000.
  - R&D in III-V device and MMIC fabrication and technology
  - Involved in development of unit processes in fabrication like wet & dry etching, ohmic contact formation, ion implant activation, rapid thermal annealing, electroplating, interconnect formation, wafer thinning, die & wire bonding and packaging, reliability testing, and wafer & device characterization.
- Team member to implement 0.7 and 0.5 micron MESFET based technologies for production of MMICs.
- Team member to develop 0.5 micron pHEMT devices and MMIC technologies
- Team member to develop GaAs-based RF MEMS devices

Publications:

Journal papers

1. "Evolution of surface morphology of alloyed AuGe/Ni/Au ohmic contacts to GaAs microwave FETs,", **G. Sai Saravanan**, K. Mahadeva Bhat, S. Dhamodaran, A.P. Pathak, R. Muralidharan, H.P. Vyas, D. V. Sridhara Rao, R. Balamuralikrishnan and K. Muraleedharan, Material Science in Semiconductor Processing, 30 (2015) 62–74.
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3. "Design and Electrical Characterization of Wafer-level Micro-package for GaAs-based RFMEMS Switches," Sandeep Chaturvedi, **G. Sai Saravanan**, Mahadeva K. Bhat, Sangam Bhalke, S. L.

Badnikar, R. Muralidharan and Shiban K. Koul, IETE journal of research, Vol.59 (3), May-Jun 2013, 201-209

4. "Gate recess structure engineering using silicon-nitride-assisted process for increased breakdown voltage in pseudomorphic HEMTs," K Mahadeva Bhat, Saptarshi Mandal, Saptarshi Pathak, **G Sai Saravanan**, Ch Sridhar, S L Badnikar, H P Vyas, R Muralidharan, M K Jain and A Subrahmanyam, Semiconductor Science and technology, 2012, Vol. 27, 115013
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6. "Electromagnetic simulation and characterization of a metal ceramic package for packaging of high isolation switches," S. Chaturvedi, S. V. Bhalke, and **G. Sai Saravanan**, Progress In Electromagnetics Research C, Vol. 16, 111-125, 2010
7. "Ohmic contacts to pseudomorphic HEMTs with low contact resistance due to enhanced Ge penetration through AlGaAs layers," **G. Sai Saravanan**, Mahadeva Bhat. K, K. Muraleedharan, H. P. Vyas, R. Muralidharan and A. P. Pathak, Semiconductor Science and technology, 2008, Vol. 23, 501-6, 025019.
8. "Influence of activation of Si29+ ion-implantation in GaAs on ohmic contact resistance and electrical performances of MESFETs," **G. Sai Saravanan**, Mahadeva Bhat. K, H. P. Vyas, K. Muraleedharan and A. P. Pathak, Radiation effects & defects in solids, Vol. 163, No. 9, September 2008, 737–748.
9. "Swift heavy ion irradiated InGaAs/InP multi quantum wells: Band structure, interface and surface modifications," S. Dhamodaran, A. P. Pathak, A. Turos, **G. Sai Saravanan**, S. A. Khan, D. K. Awasti and B. M. Arora, Nuclear Instruments and Methods in Physics Research B, 266, 2008, 583-588.
10. "Ion beam modification of strained InGaAs/InP characterized by HRXRD, PL and AFM," G Devaraju, S Dhamodaran, AP Pathak, **G. Sai Saravanan**, J Gaca, M Wojcik, A Turos, SA Khan, DK Avasthi, BM Arora, Nuclear Instruments and Methods in Physics Research B, 266, 2008, 3552-3556.
11. "Transmission electron microscopy characterization of electronic materials and device structures," D. V. Sridhara Rao, **G. Sai Saravanan**, K. Muraleedharan, R. Balamuralikrishnan, R. Muralidharan and H. P. Vyas, Metals, Materials and Processes, 2007, Vol. 19, No. 1-2, 171-80.
12. "Low- and high-energy irradiations of InGaAs /GaAs heterostructures: a comparison," S. Dhamodaran, A. P. Pathak, D. K. Awasti, R. Muralidharan, **G. Sai Saravanan**, B. Sundaravel, R. Kesavamurthy and K. G. M. Nair, Radiation effects and defects in solids, Vol. 162, Nos. 3-4, 2007, 215-221.
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15. "Fabrication of mm-wave Gunn and IMPATT devices with IHS – IBR: a new approach," Ishwar Chandra, R. Gulati, H.S. Sharma, S. Mohan, A.A. Naik, **G. Sai Saravanan**, Materials Science and Engg. B, Vol. B28, 1994, pp. 253-256

International Conferences and Workshops

1. "MESFET Process Based Planar Schottky Diode and its application to Passive Power Limiters," Sandeep Chaturvedi, **G. Sai Saravanan**, Mahadeva Bhat. K., Sangam V. Bhalke, Dec 2013, IMARC, New Delhi
2. "Electron microscopy study of AuGe/Ni/Au ohmic contacts to GaAs MHEMT structure," Mahadeva Bhat K, D.V. Sridhara Rao, **G. Sai Saravanan**, H.P.Vyas, S.L.Badnikar, R. Muralidharan, M.K. Jain, A.Subrahmanyam, International conference on Electron Nanoscopy, Hyderabad, India, July 6-8, 2011
3. "RBS, XRD, Raman and TEM studies on Ge nanocrystals embedded in SiO2 prepared by Atom Beam Sputtering," N Srinivasa Rao, Anand P Pathak, N Sathish, G Devaraju, V Saikiran, **G. Sai Saravanan**, D K Avasthi, and D Kabiraj, 17th International Conference on Ion Beam Modification of Materials, Montreal, Aug. 22-27, 2010
4. "Backside SIMS Analysis and Accelerated Thermal Aging of Optimally Alloyed Ohmic Contacts to MESFETs," **G. Sai Saravanan**, Mahadeva Bhat K, Sandeep Chaturvedi, M.N. Mudholkar, R. Muralidharan, CS MANTECH, May 17-20, 2010, Portland, USA
5. "EM Simulation and Development of Wafer Level Micro-packaging Technique for GaAs-based RFMEMS Switches," Sandeep Chaturvedi, Sangam V. Bhalke, Mahadeva Bhat. K., **G. Sai Saravanan**, R. Muralidharan, Shiban K. Koul, CS MANTECH, May 17-20, 2010, Portland, USA
6. "Enhancement of Uniformity of Activation and Electrical Parameters in GaAs Wafers by Reduction of Slip Lines during Rapid Thermal Processing," **G. Sai Saravanan**, Mahadeva Bhat. K, Bishakha Bhattacharya, M.N. Mudholkar and R. Muralidharan, IWPSD 2009, New Delhi
7. "Gate lift-off process by single photoresist layer using developer soaking," Ch. Sridhar, Mahadeva Bhat, AVSK. Rao, **G. Sai Saravanan**, R. Muralidharan, IWPSD 2009, New Delhi
8. "Simulation of carrier concentration and electric field between gate and drain in GaAs MESFETs using finite element method," Saptarshi Mandal, Mahadeva Bhat K, **G. Sai Saravanan**, R Muralidharan, R.Sankarasubramanian, IWPSD 2009, New Delhi
9. "New planarization method for fabrication of GaAs RF MEMS with improved yield," Mahadeva Bhat, **G. Sai Saravanan**, Ramjay Pal, P. Datta, R. Muralidharan, IWPSD 2009, New Delhi
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14. "A Study on Variation of Equivalent Circuit Parameters of Pseudomorphic HEMT Switch with number of Gate Fingers," Samarth Mittal, Amit Kumar Verma, Sandeep Chaturvedi, Mahadeva Bhat. K., **G. Sai Saravanan**, R. Muralidharan, ISMOT 2009, New Delhi
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18. “Effect of variation of topological changes on the equivalent circuit parameters of pseudomorphic HEMTs,” B. Naveen Kumar, Gaurav Srivastava, Amit Kumar Verma, Mahadeva Bhat K, Sandeep Chaturvedi, **G. Sai Saravanan**, R. Muralidharan, Int. IEEE Conf. ELECTRO-2009, IT-BHU, Varanasi, India, Dec. 2009.

19. “Optimization of pulse reversal electrodeposition with fine grains and low roughness for GaAs RF MEMS structures”, **G. Sai Saravanan**, Mahadeva Bhat, S. Dattatreya Prasad, Sandeep Chaturvedi, R. Muralidharan, S. Dhamodaran, and, N. Sathish, presented in IEDST 2009 (June 1-2, 2009 at IIT, Mumbai)

20. “Gate recess structure engineering in MESFETs to achieve higher schottky breakdown voltage for switch MMIC applications,” Mahadeva Bhat K, **G. Sai Saravanan**, H.P.Vyas, M.K. Jain, A.Subrahmanyam, R. Muralidharan, presented in IEDST 2009 (June 1-2, 2009 at IIT, Mumbai)

21. “Bias dependent scalable signal modeling of pseudomorphic HEMTs”, Amit Kumar Verma, Sandeep Chaturvedi, Mahadeva Bhat K., **G. Sai Saravanan**, Dr. R.Muralidharan, presented in IEDST 2009 (June 1-2, 2009 at IIT, Mumbai)

22. “A low loss S-band 6-bit GaAs MMIC Digital Attenuator with High Attenuation Accuracy,” Amit Prabhat Singh Yadav, Vijesh Arora, Sangam Bhalke, Sandeep Chaturvedi, **G. Sai Saravanan**, Mahadeva Bhat.K., R. Muralidharan, Jan 2009

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29. "Influence of oxygen plasma treatment on the uniformity of activation of rapid thermal annealed GaAs wafers," **G. Sai Saravanan**, M.N. Mudholkar, Mahadeva Bhat K, Vijay V. Subraveti, AVSK Rao, K. Muraleedharan, A.P. Pathak and H.P. Vyas, 2005 Proc. of 13th Int. Workshop on Physics of Semiconductor Devices, (New Delhi, India) p 852 – 6.

30. "Pulse reversal electrodeposition for fine-grained structure and superior wire bond strength in metallisation of MMICs," **G. Sai Saravanan**, Sandeep Chaturvedi, S. D. Prasad, Sangam Bhalke, K. Muraleedharan, H. S. Sharma, and H. P. Vyas, presented in 13th Int. Workshop of Physics of Semiconductor Devices, New Delhi, 2005, pp. 847-851.

31. "Study Of Dry Etching Process To Yield Smooth Etched Surface/Side Walls For Reliable Via-Hole Ground Connections in GaAs MMICs", D.S. Rawal, V.R. Agarwal, H.S. Sharma, **G. Sai Saravanan**, B.K. Sehgal, R. Gulati, H.P. Vyas, Kishan, P. Suryanarayana, A.V.S.K. Rao, P.A. Govindacharyulu, 12th IWPSD Proceedings, K.N. Bhat and A. Das Gupta, Editors, Vol.-2, p. 809, Chennai, India (2003).

32. "Engineering of gate recess structure to obtain high VB in GaAs MESFETs", Mahadeva Bhat, **G. Sai Saravanan**, R.K. Khatri, A.V.S.K. Rao, P. Suryanarayana, Rajesh Kumar, P.A. Govindacharyulu & H.P. Vyas, 13th AGM-MRSI & these symposium on 'Perspectives in materials characterisation', Feb. 07-09, 2002, Hyderabad.

33. "Process optimization of the polyimide capacitors used for GaAs MMICs", V.G. Saravanan, Rajesh Kumar, A.N. Kishan Kona, P. Suryanarayana, Mahadeva Bhat, **G. Sai Saravanan**, A.V.S.K. Rao, P.A. Govindacharyulu, 13th AGM-MRSI & these symposium on 'Perspectives in materials characterisation', Feb07-09, 2002, Hyderabad.

34. "Fabrication and Characterisation of 200μm Deep, Dry Etched Via Holes for GaAs MMICs" D.S. Rawal, V.R. Agarwal, H.S. Sharma, **G. Sai Saravanan**, A. Pandey, S.R. Shukla, R. Sharma, A. Kumar, U.C. Ray, A. Agarwal, R. Kumar, S. Prasad, P. Suryanarayana and A.V.S.K. Rao, 11th IWPSD, Proceedings of SPIE, V. Kumar and P.K. Basu, Editors, Vol.-2, p.1034, New Delhi, India, Jan 2002.

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41. “A high yield lift-off process for interconnect formation for mm-wave beam lead Schottky diodes,” B.K. Sehgal, Sindhu Dayal, D.S. Rawal, **G. Sai Saravanan**, R. Gulati, Ishwar Chandra, Proc. 8th Int. Workshop of Physics of Semiconductor devices, Dec. 1995, N. Delhi, pp. 184.
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